REMARKS

The application has been reviewed in light of the final Office Action dated January 12, 2005. Claims 1-11 are pending, with claim 1 being the sole claim in independent form which is under examination. Claims 12-22 were withdrawn by the Patent Office from examination. By this Amendment, claims 12-22 have been canceled without prejudice or disclaimer, and claim 1 has been amended to clarify the claimed invention. No new matter has been introduced by this Amendment. Support for the claim amendments can be found in the application at, for example, page 27, line 24 through page 28, line 11, page 33, line 24 through page 34, line 23, and page 63, line 15 through page 64, line 9.

The title of the invention was objected to as purportedly not descriptive.

By this Amendment, the title has been amended.

Withdrawal of the objection to the title is respectfully requested.

Claims 1 and 7 were rejected under 35 U.S.C. §102(b) as purportedly anticipated by U.S. Patent No. 4,783,738 to Li et al. Claims 1 and 7-9 were rejected under 35 U.S.C. §102(b) as purportedly anticipated by U.S. Patent No. 5,430,885 to Kaneko et al. Claim 1 was rejected under 35 U.S.C. §102(a) as purportedly anticipated by Applicant's Admitted Prior Art. Claim 2 was rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Li. Claims 3, 4, 8 and 9 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Li in view of Kaneko. Claims 5, 6, 10 and 11 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Li in view of Patterson et al., "Computer Architecture - A Quantitative Approach", (2nd Edition 1996). Claims 2-4 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Kaneko. Claims 5, 6, 10 and 11 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Kaneko in view of Patterson.

Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit that independent claim 1 is patentable over the cited art, for at least the following reasons.

This application relates to a parallel processor and/or image processing apparatus adapted for nonlinear processing. The application describes a feature which allows assorted SIMD (single instruction stream multiple data stream) instructions as well as non-linear processing to be performed efficiently.

For example, claim 1 of the present application is directed to a parallel processor comprising a global processor and a processor-element block comprising a plurality of processor elements. The global processor interprets a program and controls the entirety of the parallel processor. Each processor element comprises a register file and an operation array for processing a plurality of sets of data. The global processor assigns to the processor elements respective processor-element numbers, and can output a control signal to the processor elements to set the assigned processor-element numbers corresponding to the processor elements as input values of the operation arrays, respectively. In addition, the claimed invention of amended claim 1 includes the feature that for each processor element the register file of the processor element holds plural sets of data for operation processing by the operation array of the processor element, according to processor element instructions from the global processor. Thus, the global processor can instruct selected processor elements to perform non-linear processing, while reducing the number of instruction execution cycles.

The background art described in the Description Of Related Art section of the application does not disclose such features. For example, the related art mentioned at page 11, lines 2-17 requires instructions for non-linear processing to be loaded serially, that is, shifted in bit-by-bit.

In contrast, the claimed invention of claim 1 allows processor element numbers to be set by a single instruction, and then operation processing can proceed selectively by an instruction from the global processor loaded from a bus.

The other cited references likewise do not disclose or suggest the claimed invention.

Li, as understood by Applicants, is directed to an instruction adapter for processing elements of an array processor. Each processing element has a PID register which can be preloaded with a PID for the processing element. It is contended in the Office Action that each processing element includes multiple registers which collectively constitute a register file.

Applicants do not find teaching or suggestion in Li, however, that each processing element has a register file which holds plural sets of data for operation processing by the operation array of the processor element, according to processor element instructions from the global processor, as provided by the claimed invention of amended claim 1. The registers of Li are provided for the processing of instructions from the array controller.

Kaneko, as understood by Applicants, is directed to a multi-processor system for multi-dimensional image signal processing, including a host processor and plural co-processors. Kaneko discloses that each co-processor (PE) has an inherent PE number, so that the co-processors can carry out different tasks and can communicate with the host processor. It is contended in the Office Action that each co-processor inherently includes a register file and an operation array.

Applicants do not find teaching or suggestion in Kaneko, however, that each processing element has a register file which holds plural sets of data for operation processing by the operation array of the processor element, according to processor element instructions from the global processor, as provided by the claimed invention of amended claim 1.

Contrary to the contention in the Office Action, the processing element does not have to have a register file. For example, processing elements in a multi-processor system such as the system of Kaneko can include a register scheme whereby only a single set of data is held for operation processing. As well-established by the relevant case law, a feature is inherent to a reference only if it must necessarily be present and one skilled in the art would recognize its presence [see, for example, Crown Operations Int'l Inc. v. Solutia Inc., 289 F.3d 1367, 1377, 62 U.S.P.Q.2d 1917 (Fed.Cir. 2002)].

Patterson is cited in the Office Action as purportedly disclosing using a general purpose register to specify a pointer, and incrementing the contents of the register after the specifying.

Applicants do not find disclosure or suggestion by the cited art, however, of a parallel processor comprising a global processor and a processor-element block comprising a plurality of processor elements, wherein the global processor assigns to the processor elements respective processor-element numbers and can output a control signal to the processor elements to set the assigned processor-element numbers corresponding to the processor elements as input values of the operation arrays, respectively, and for each processor element the register file of the processor element holds plural sets of data for operation processing by the operation array of the processor element, according to processor element instructions from the global processor, as provided by the claimed invention of amended claim 1.

Accordingly, for at least the above-stated reasons, Applicants respectfully submit that independent claim 1, and the claims depending therefrom, are patentable over the cited art.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our

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If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Allowance of this application is respectfully requested.

Respectfully submitted,

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